

WHAT IS CLAIMED IS:

- 1 1. Apparatus having an interface port for simultaneously
2 transmitting and receiving input and output signals,
3 comprising:
4 a first circuit for generating an output signal;
5 a second circuit having a first terminal and a second
6 terminal, the first terminal coupled to the first circuit, the
7 second terminal coupled to the interface port, a signal level
8 at the first terminal representing a first combination of the
9 input and output signals, and a signal level at the second
10 terminal representing a second combination of the input and
11 output signals; and
12 a third circuit coupled to the first and second terminals
13 of the second circuit for determining the input signal based
14 on the signal levels at the first and second terminals.
- 1 2. The apparatus of Claim 1, wherein the second circuit
2 comprises a resistor, the first terminal comprises a first end
3 of the resistor, and the second terminal comprises a second
4 end of the resistor.
- 1 3. The apparatus of Claim 1, wherein the third circuit
2 processes the first and second combinations of the input and
3 output signal levels to generate a signal that corresponds to
4 the input signal.

1 4. The apparatus of Claim 1, wherein the third circuit
2 multiplies the first combination of the input and output
3 signal levels by a first constant to generate a first number
4 and multiplies the second combination of the input and output
5 signal levels by a second constant to generate a second
6 number, the difference between the second and the first
7 numbers corresponding to the input signal.

1 5. The apparatus of Claim 4, wherein the interface port is
2 coupled to a transmission line having an impedance of Z, the
3 second circuit has a resistance of Ra, and the ratio between
4 the first constant and the second constant is approximately
5 equal to $Z / (Z + Ra)$.

1 6. The apparatus of Claim 4, wherein the interface port is
2 coupled to a transmission line having an impedance of Z via a
3 resistance of Rc, the interface port being coupled to electric
4 ground via a resistance of Rb, the second circuit having a
5 resistance of Ra, and the ratio between the first constant and
6 the second constant being approximately equal to
7 $Rb * (Z + Rc) / (Rb * (Z + Rc) + Ra * (Rb + Rc + Z))$.

1 7. An integrated circuit comprising:
2 a first circuit for providing a variable output signal;

3 an internal impedance having a first terminal and a
4 second terminal, the first terminal electrically connected to
5 the first circuit;

6 an interface port electrically connected to the second
7 terminal of the internal impedance, a signal level at the
8 interface port corresponding to a combination of the variable
9 output signal and an input signal from an external circuit;
10 and

11 a second circuit for processing the signal levels at the
12 first and second terminals at the internal impedance to
13 generate a signal that corresponds to the input signal from
14 the external circuit.

1 8. The apparatus of Claim 7, wherein the second circuit
2 multiplies a signal level at the first terminal of the
3 internal impedance by a first constant to generate a first
4 number and multiplies a signal level at the second terminal of
5 the internal impedance by a second constant to generate a
6 second number, the difference between the second and the first
7 numbers corresponding to the input signal.

1 9. The apparatus of Claim 8, wherein the interface port is
2 coupled to a transmission line having an impedance of Z , the
3 second circuit has a resistance of R_a , and the ratio between

4 the first constant and the second constant is approximately
5 equal to $Z / (Z + Ra)$.

1 10. The apparatus of Claim 8, wherein the interface port is
2 coupled to a transmission line having an impedance of Z via a
3 resistor having a resistance of Rc , the interface port being
4 coupled to electric ground via a resistance of Rb , the second
5 circuit having a resistance of Ra , and the ratio between the
6 first constant and the second constant being approximately
7 equal to $Rb (Z + Rc) / (Rb (Z + Rc) + Ra (Rb + Rc + Z))$.

1 11. A system comprising:
2 a transmission line having a first end and a second end;
3 a first driver for generating a first output signal;
4 a first bridge having a first terminal for coupling to
5 the first driver and a second terminal for coupling to the
6 first end of the transmission line;
7 a second driver for generating a second output signal;
8 a second bridge having a first terminal for coupling to
9 the second driver and a second terminal for coupling to the
10 second end of the transmission line;
11 a first arithmetic unit for processing signal levels of
12 the first and second terminals of the first bridge to generate
13 a first computed signal that corresponds to the second output
14 signal; and

15 a second arithmetic unit for processing signal levels of
16 the first and second terminals of the second bridge to
17 generate a second computed signal that corresponds to the
18 first output signal.

1 12. The system of Claim 11, wherein the first bridge
2 comprises a first resistor, the first terminal of the first
3 bridge comprises a first end of the first resistor, the second
4 terminal of the first bridge comprises a second end of the
5 first resistor, the second bridge comprises a second resistor,
6 the first terminal of the second bridge comprises a first end
7 of the second resistor, and the second terminal of the second
8 bridge comprises a second end of the second resistor.

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1 13. The system of Claim 11, wherein the first arithmetic unit
2 multiplies a signal level at the first terminal of the first
3 bridge by a first constant to generate a first number and
4 multiplies a signal level at the second terminal of the first
5 bridge by a second constant to generate a second number, the
6 difference between the second and the first numbers
7 corresponding to the input signal.

1 14. The system of Claim 13, wherein the transmission line has
2 an impedance of Z , the first bridge has a resistance of R_a ,
3 and the ratio between the first constant and the second
4 constant is approximately equal to $Z / (Z + R_a)$.

1 15. The apparatus of Claim 13, wherein the transmission line
2 has an impedance of Z, the first bridge has a resistance of
3 Ra, the second terminal of the first bridge is coupled to
4 electric ground via a resistance of Rb, the second terminal of
5 the first bridge is coupled to the transmission line via a
6 resistance of Rc, and the ratio between the first constant and
7 the second constant is approximately equal to
8 $Rb * (Z + Rc) / (Rb * (Z + Rc) + Ra * (Rb + Rc + Z))$.

1 16. A memory chip comprising:
2 an interface pin for simultaneously reading in write data
3 to the memory chip and sending out read data from the memory
4 chip;
5 a driver for generating the read data;
6 an internal impedance having a first and a second
7 terminals, the first terminal being electrically coupled to
8 the driver and the second terminal being electrically coupled
9 to the interface pin; and
10 an arithmetic unit for processing signal levels of the
11 first and second terminals of the internal impedance and for
12 generating a signal corresponding to the write data.

1 17. The memory chip of Claim 16, wherein the arithmetic unit
2 multiplies a signal level at the first terminal by a first
3 constant to generate a first number and multiplies a signal

4 level at the second terminal by a second constant to generate
5 a second number, the difference between the second and the
6 first numbers corresponding to the write data.

1 18. The memory chip of Claim 16, wherein the interface pin is
2 coupled to a transmission line having an impedance of Z , the
3 internal impedance has an impedance of R_a , and the ratio
4 between the first constant and the second constant is
5 approximately equal to $Z / (Z + R_a)$.

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1 19. The memory chip of Claim 16, wherein the interface pin is
2 coupled to a transmission line having an impedance of Z via a
3 resistance of R_c , the interface pin being coupled to electric
4 ground via a resistance of R_b , the internal impedance having
5 an impedance of R_a , and the ratio between the first constant
6 and the second constant being approximately equal to
7 $R_b * (Z + R_c) / (R_b * (Z + R_c) + R_a * (R_b + R_c + Z))$.

1 20. A system comprising:
2 a data bus having a first end and a second end;
3 a processor for generating write data, the processor
4 having a first interface port and a first arithmetic unit, the
5 first interface port being coupled to the first end of the
6 data bus; and
7 a memory for generating read data, the memory having a
8 second interface port and second arithmetic unit, the second

9 interface port being electrically coupled to the second end of
10 the data bus;

11 wherein the write data is sent from the processor to the
12 memory via the data bus at the same time that the read data is
13 sent from the memory to the processor via the data bus, the
14 first arithmetic unit processing combinations of the write and
15 read data to generate a first computed signal corresponding to
16 the read data, and the second arithmetic unit processing
17 combinations of the read and write data to generate a second
18 computed signal corresponding to the write signal.

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1 21. The system of Claim 20, wherein the processor further
2 comprises a first driver and a first bridge, the first driver
3 generating the write data, the first bridge having a first
4 terminal coupled to the first driver and a second terminal
5 coupled to the first end of the data bus, the first arithmetic
6 unit processing the signal levels at the first and second
7 terminals of the first bridge to generate the first computed
8 signal.

1 22. The system of Claim 21, wherein the first arithmetic unit
2 multiplies the signal level at the first terminal of the first
3 bridge by a first constant to generate a first number and
4 multiplies the signal level at the second terminal of the
5 first bridge by a second constant to generate a second number,

6 the difference between the second and the first numbers
7 corresponding to the read signal.

1 23. The system of Claim 20, wherein the memory further
2 comprises a second driver and a second bridge, the second
3 driver generating the read signal, the second bridge having a
4 first terminal coupled to the second driver and a second
5 terminal coupled to the second end of the data bus, the second
6 arithmetic unit processing the signal levels at the first and
7 second terminals of the second bridge to generate the second
8 computed signal.

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1 24. The system of Claim 23, wherein the second arithmetic
2 unit multiplies the signal level at the first terminal of the
3 second bridge by a third constant to generate a third number
4 and multiplies the signal level at the second terminal of the
5 second bridge by a fourth constant to generate a fourth
6 number, the difference between the fourth and the third
7 numbers corresponding to the write signal.

1 25. A system comprising:
2 a data bus having a first end and a second end;
3 a first device comprising:
4 a first driver for generating a first output signal,

5 a first bridge having a first terminal for coupling
6 to the first driver and a second terminal for coupling to the
7 first end of the data bus, and

8 a first arithmetic unit; and

9 a second device comprising:

10 a second driver for generating a second output
11 signal,

12 a second bridge having a first terminal for coupling
13 to the second driver and a second terminal for coupling to the
14 second end of the data bus, and

15 a second arithmetic unit;

16 wherein the first arithmetic unit processes signal levels
17 of the first and second terminals of the first bridge to
18 generate a first computed signal that corresponds to the
19 second output signal, and the second arithmetic unit processes
20 signal levels of the first and second terminals of the second
21 bridge to generate a second computed signal that corresponds
22 to the first output signal.

1 26. The system of Claim 25, wherein the first device is a
2 computer.

1 27. The system of Claim 26, wherein the second device is a
2 disk drive.

1 28. The system of Claim 26, wherein the second device is an
2 input/output device.

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